SI-MONOLITHIC MICROWAVE PRESCALER IC

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ABSTRACT

This paper describes a Si Monolithic microwave Prescaler IC with a toggle frequency of 3.9 GHz. To optimize circuit parameters and to determine the dominant transistor parameters, precise computer simulation has been used.
An improved IC manufacturing process was developed to achieve the desired parameters and to obtain a transistor cut-off frequency of 10 GHz.

MICROWAVE PRESCALER IC

In the design of microwave local oscillators for recent digital microwave equipment, automatic phase control technique using a digital frequency divider has been the most suitable solution for frequency stability and analog service channel transmission from the local oscillator(1). A prescaler IC operating in the 1 GHz frequency range is commercially available, but it requires a relatively large 1 GHz VCO and frequency multipliers. A microwave prescaler IC operating in the C-band is a high priority requirement for microwave local oscillator designers.
A typical microwave prescaler consists of a master-slave flip-flop circuit (2), To raise the prescaler toggle frequency, not only improvements in the IC manufacturing process but also circuit parameter optimization is highly desirable.

COMPUTER-AIDED CIRCUIT DESIGN

The fundamental circuit of this prescaler consists of a master and slave flip-flop, as shown in Fig. 1.
Prescaler simulation requires a great deal of computing time, for the following reasons:

(A) prescaler simulation relies on transient analysis or iterative calculations, not on frequency response analysis.
(B) One pulse analysis is not enough to verify perfect prescaler operation since miscounting occasionally occurs, as shown in Fig. 2.
(C) Without special initialization, the prescaler can not operate immediately, as shown in Fig. 3.
(D) One analysis demonstrates only if the prescaler can operate at one particular frequency.

To optimize circuit and transistor parameters much more precisely, pulses at internal nodes are simulated and compared. The master and slave flip-flops are initially set to opposite states using SPICE code ".IC", and the prescaler can operate immediately. A precise wave form can be simulated with this method, as shown in Fig. 4. The following results have been found:

(A) To receive data more rapidly from the other flip-flop, the collector-to-substrate capacitance of transistor Q6 ,Q7 or the collector load resistance R11 must be reduced. The slope indicated by the arrow in Fig.4 increases as these are reduced.
(B) Additional capacitance CB in Fig. 1 synchronizes the current switch symmetrically with the input clock, as shown in Fig. 4 (without CB) and Fig. 5 (with CB).

The clock frequencies in Fig. 3,4 and 5 are 2.5 GHz; half a pulse section is 200 pS. Horizontal time scales are 500 pS/division for Fig.2 ,1nS/division for Fig. 3 and 400 pS/division for Fig.4,5. Left voltage scale (1V/division) is for the voltage waveform node 26 to 29 and 32. Right voltage scale (5uV/division) is for the voltage waveform between node 23 and 230, or between node 24 and 240. These internodal waveforms show the current which flows through an imaginary 0.001 ohm resistor (ie. 5mA/division) , and indicates current switch operation.

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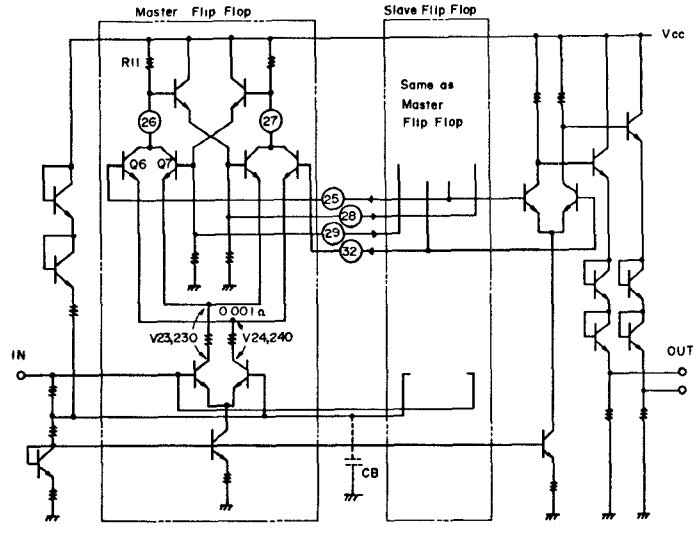

Fig. 1 Master-slave flip-flop circuit.

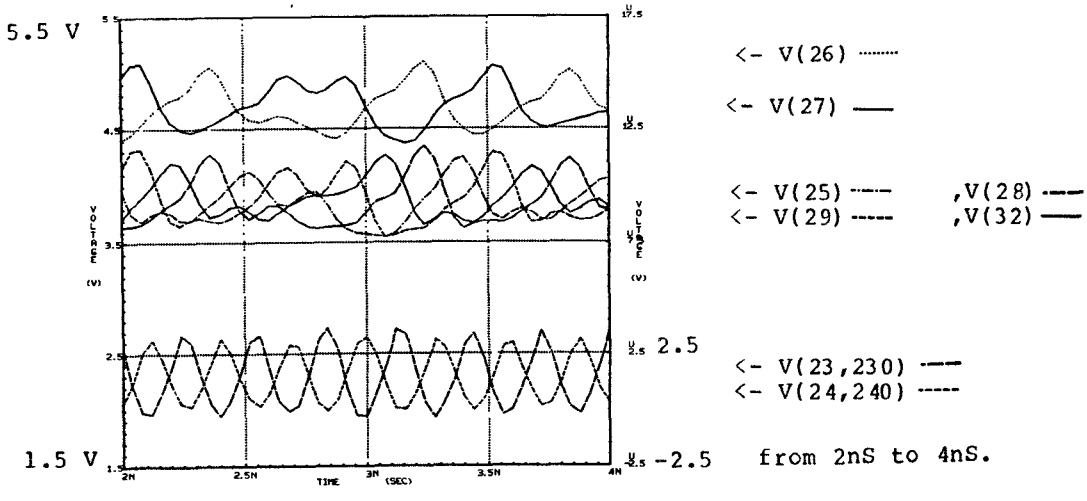

Fig.2 Simulated Waveform of Miscounting (3.4GHz).

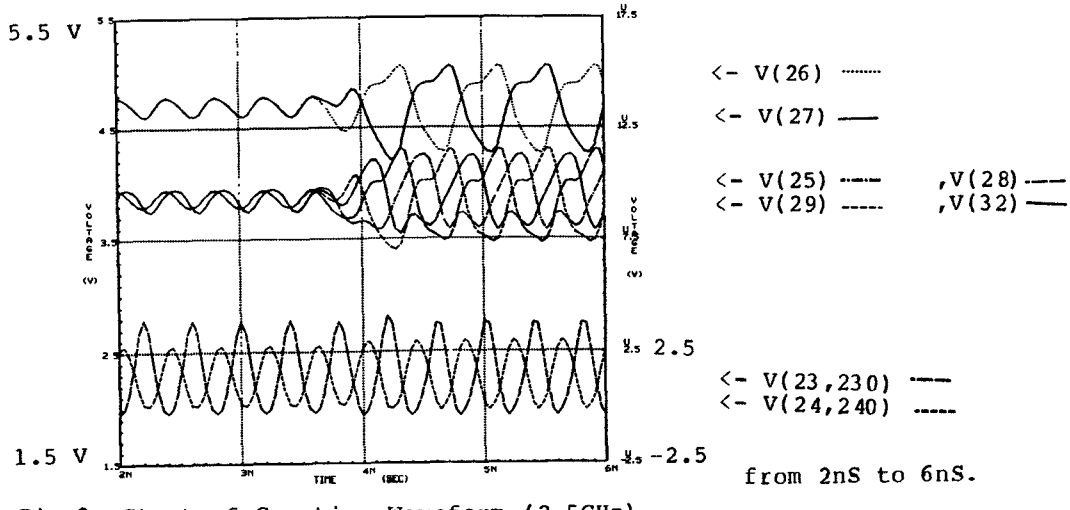

Fig.3 Start of Counting Waveform (2.5GHz).

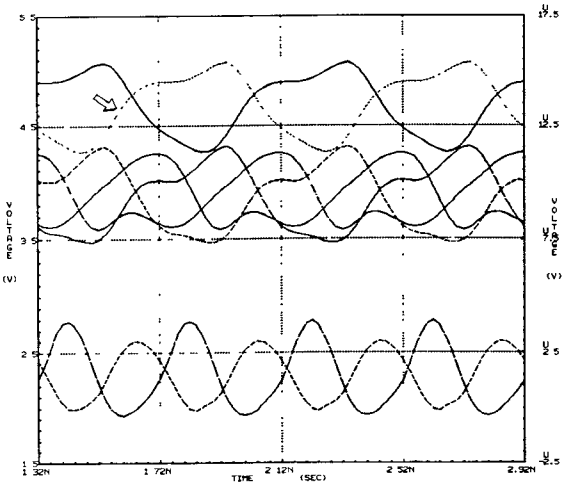

Fig.4 Precise Waveform without CB (2.5GHz).

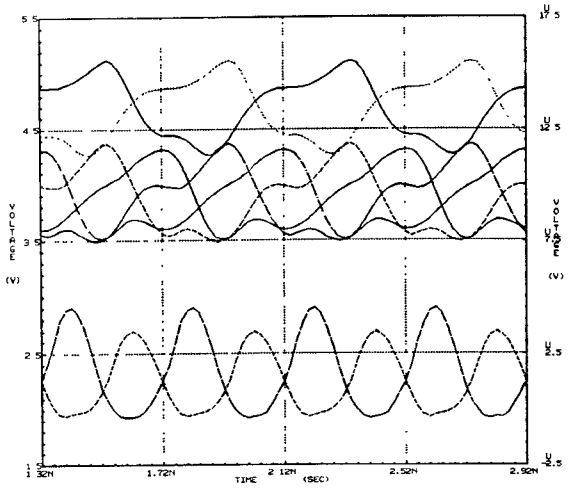

Fig.5 Precise Waveform with CB (2.5GHz).

PROCESS DESIGN

Several Si monolithic bipolar IC processes have been reported, most notably SST-1A (3) and APSA (4). A Si microwave monolithic IC process without self-alignment method, has also been reported (5). This process is called DNP-I (Direct Nitride Passivated base surface -I) and is capable of producing a transistor with a cut-off frequency of 6.5 GHz.

To achieve the transistor parameters determined by the computer simulation studies, the DNP-I process has been enhanced and is herein after referred to as a DNP-II process. This enhanced process has the following features:

(A) To reduce parasitic capacitance, oxide isolation is applied, and a smaller buried layer is selected.
(B) To achieve ft= 10 GHz, a shallow base (Xjc=0.2μm) is formed by ion implantation and lamp-anealing. A shallow emitter (Xje=0.1μm) is formed by diffusion from As-doped polysilicon.
(C) To reduce base resistance and E-B junction capacitance, an emitter of 1 um width is formed.
(D) To facilitate pattern design and form highly reliable electrodes, a Ti-Pt-Au electrode structure is employed.
(E) To achieve an extremely high reliability, the base surfase is covered by an additional nitride film after the thin oxide film is applied.

A cross sectional view of a DNP-II transistor cell is shown in Fig. 6. Table 1 compares the profiles produced by DNP-I and DNP-II processes. In the case of the DNP-II profile a great contraction in pattern rule was obtained and the base and collector regions are reduced to less than 60 % . Table 2 compares the performance of transistors produced by DNP-I and DNP-II processes.

RESULTS

A die photograph is shown in Fig. 7 which includes the tandem two-stage master slave flip-flop from Fig.1. Additional capacitor CB is composed of a buried layer and electrode; resistors are P+ polysilicon.

Operating waveforms at 3.3 GHz are shown in Fig. 8. The maximum operating frequency of 3.9 GHz has been achieved at a power dissipation of 316 mW and a supply voltage of 5 V.

CONCLUSION

A prescaler IC operating up tp 3.9 GHz has been developed. This IC will be useful for the size reduction of microwave local oscillators.

This new IC process, based on the latest discrete microwave transistor process, is applicable to other microwave monolithic ICs.

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Table 1. Basic Transistor Profile Comparison.

item	DNP-I	DNP-II
Emitter width	1μm	1μm
Emitter length	40x4μm	40X4μm
Base area	2904μm**2	1596μm**2
Collector area	4968μm**2	2880μm**2
Electrode width	5μm	2μm
Electrode interval	2.5μm	2μm
Epitaxial thickness	1.5μm	1.5μm

Table 2. Transistor Performance Comparison.

Parameter	DNP-I	DNP-II
BVcbo	25V	25V
BVceo	12V	12V
BVebo	4V	3V
hFE	100	100
fT	6.5GHz	10GHz

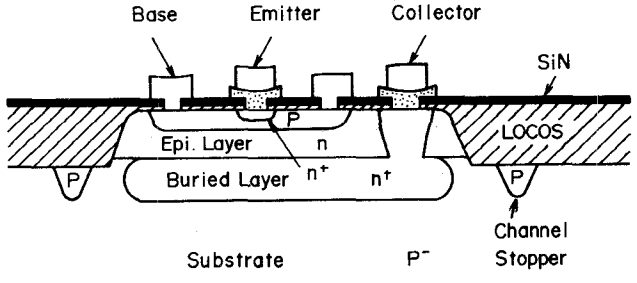

Fig. 6 A cross sectional view of transistor cell.

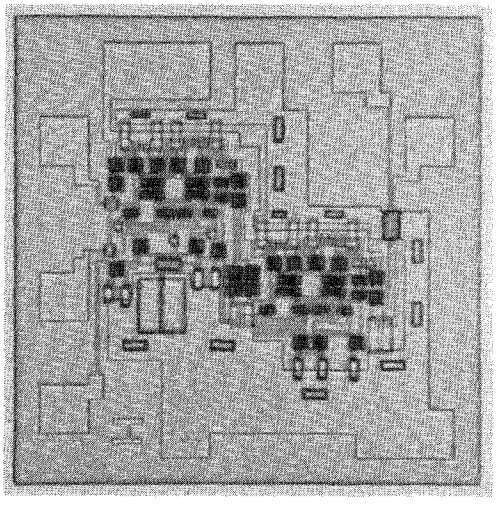

Fig.7 Die Photograph.

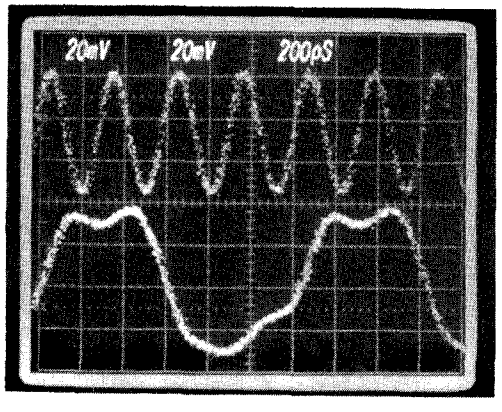

Fig. 8 Measured input output waveforms of an 1/4 divider for a 3.3 GHz sinusoidal clock.

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